Mazda 46V

Low VOC Chip Repair Process

Technical Bulletin
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The chip repair process outlined in this document is necessary to meet appearance, performance, and regulatory requirements. Contact your PPG representative for full documentation on the approved products, systems and processes. The repair process below is designed for Low VOC Compliant area.

PREPARATION OF REPAIR AREA:

- Wash vehicle with soap and water and dry thoroughly
- Wipe area to be repaired with appropriate ONECHOICE® SX wax and grease remover.
  - Refer to P-Sheet OC-42. Link
- Prep vehicle and featheredge chipped area.
- Blow off area with compressed air and re-clean with appropriate *OneChoice* SX Low VOC cleaner.
- If any bare metal substrate is visible, apply *OneChoice* SX1071 ECOBASE™ 5.5 Etch Prime as directed per P-Sheet OC-6.
  - . Link
- Apply ENVIROBASE® High Performance ECP11/15/17 A-Chromatic Surfacer or AQUABASE® Plus P565-5401/5405/5407 HS Plus Primer Surfacer to the repair area as per their respective P-Sheets.
  - . Link (*Envirobase* High Performance)
  - . Link (*Aquabase* Plus)

If applying a primer sealer to the repair, or for panel replacement on properly prepared ecoat, use *Envirobase* Plus ECS21/25/27 A-Chromatic LV Sealers or *Aquabase* Plus P565-3121/3125/3127 HS Plus Wet on Wet Sealer as per their respective P-Sheets.

  - . Link (*Envirobase* High Performance)
  - . Link (*Aquabase* Plus)

COLOR APPLICATION:

- Apply appropriate *Envirobase* High Performance, or *Aquabase* Plus activated basecoat to the repair area.
  - Refer to *Envirobase* High Performance P-Sheet EB-143 for EHP Basecoat (with T492 & T493) Link
  - Refer to *Aquabase* Plus TDS N5.3.2 for ABP Basecoat (with P935-1250 & P935-1255) Link
- Apply Mid-Coat to achieve proper color as directed by Technical Bulletin TCB100 VM4350 Tinted Clearcoat Application Process.
  - . Link

CLEARCOAT APPLICATION:

- Apply the appropriate premium *Deltron, Envirobase* High Performance or *Aquabase* Plus clearcoat to the repair as directed by the P-Sheet.

Note: The specified process above, will provide optimum chip resistance.